LISTING OF THE CLAIMS:

1. (withdrawn) An apparatus comprising:

a package, said package comprising a plurality of shelves;

a first semiconductor die electrically coupled to at least one of said shelves; and,

a second semiconductor die electrically coupled to at least one of said shelves, wherein said second semiconductor die is above said first semiconductor die.

2. (withdrawn) The apparatus of claim 1 wherein said package comprises a ceramic pin grid array (PGA) package.

3. (withdrawn) The apparatus of claim 1 wherein said package comprises a plastic pin grid array (PPGA) package.

4. (withdrawn) The apparatus of claim 1 wherein said first semiconductor die is a central processing unit (CPU) die.

5. (withdrawn) The apparatus of claim 4 wherein said second semiconductor die is a memory cache.

6. (withdrawn) The apparatus of claim 1 wherein said package has a single chip footprint.

7. (withdrawn) The apparatus of claim 1 wherein said first semiconductor die is wire bonded to said at least one shelf.

8. (withdrawn) The apparatus of claim 7 wherein said second semiconductor die is wire bonded to said at least one shelf.

9. (withdrawn) The apparatus of claim 1 wherein said second semiconductor die is electrically attached to a substrate and said substrate is wire bonded to said at least one shelf.

10. (withdrawn) The apparatus of claim 9 wherein said second semiconductor die is wire bonded to said substrate.

11. (withdrawn) The apparatus of claim 9 wherein said second semiconductor die is electrically attached to said substrate by solder bumps.

12. (withdrawn) The apparatus of claim 1 further comprising an encapsulant filling said package above said second semiconductor die.

13. (withdrawn) The apparatus of claim 12 wherein said second semiconductor die is attached to said at least one shelf such that an open cavity protects said first semiconductor die.

14. (withdrawn) An apparatus comprising:

a plurality of shelves, said package for housing a plurality of semiconductor dies in a vertically stacked position such that said package has a single chip package footprint;

a first semiconductor die electrically coupled to at least one of said shelves; and,

a second semiconductor die electrically coupled to at least on of said shelves, wherein said second semiconductor doe as above said first semiconductor die.

15. (withdrawn) The apparatus of claim 14 wherein said package comprises a ceramic pin grid array (PGA) package.

16. (withdrawn) The apparatus of claim 14 wherein said package comprises a plastic pin grid array (PPGA) package.

17. (withdrawn) The apparatus of claim 14 wherein said first semiconductor die is a central processing unit (CPU) die.

18. (withdrawn) The apparatus of claim 17 wherein said second semiconductor die is a memory cache.

19. (withdrawn) The apparatus of claim 14 further comprising an encapsulant filling said package above said second semiconductor die.

20. (withdrawn) The apparatus of claim 19 wherein said second semiconductor die is attached to said at least one shelf such that an open cavity protects said first semiconductor die.

21. (withdrawn) A method constructing a multi-chip package, comprising:

placing a fist chip package on a first shelf;

electrically attaching said first chip package to said first shelf;

placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and,

electrically attaching said second chip package to said second shelf.

22. (withdrawn) The method of claim 21 further comprising the step of filling said package above said second chip package with an encapsulant.

23. (withdrawn) The method of claim 22 wherein said step of placing a second chip package on a second shelf further comprises placing a second chip package on a second shelf with a sealer such that a sealed open cavity below said second shelf protects said first chip package.

24. (withdrawn The method of claim 21 wherein said step of placing a first chip package further comprises placing CPU chip package on a first shelf.

25. (withdrawn) The method of claim 21 wherein said step of placing a second chip package further comprises placing a memory cache on a second shelf.

26. (withdrawn) The method of claim 21 wherein said step of electrically attaching said first chip package further comprises wire bonding said first chip package to said first shelf.27. (withdrawn) The method of claim 21 wherein said step of electrically attaching said second chip package further comprises wire bonding said second chip package to said second shelf.

28. (currently amended) A method of constructing a multi-chip package, comprising:

attaching a semiconductor die to a slug;

attaching the slug to a base of a package;

electrically connecting ~~a~~ said semiconductor die to at least one of a plurality of shelves of the package;

electrically connecting a flip-chip to a substrate; ~~and~~

attaching ~~the side of~~ said substrate ~~that does not have the flip-chip mounted to it~~ to one of said plurality of shelves~~.~~ ; and

disposing a seal between a base of said substrate and the one of said plurality of shelves to which said substrate is attached, wherein a cavity is formed between said substrate and said base of said package, the cavity comprising only said semiconductor die.

29. (previously presented) The method of claim 28, further comprising electrically connecting said substrate to at least one of said plurality of shelves.

30. (previously presented) The method of claim 29, wherein electrically connecting said substrate to at least one of said plurality of shelves comprises electrically connecting said substrate to at least one of said plurality of shelves with at least one bond wire.

31. (currently amended) The method of claim 28, wherein attaching ~~the side of~~ said substrate ~~that does not have the flip-chip mounted to it~~ to one of said plurality of shelves provides a lid above said semiconductor die.

32. (previously presented) The method of claim 28, further comprising electrically testing said electrically connected flip-chip before attaching of said substrate to said one of said plurality of shelves.

33. (previously presented) The method of claim 28, wherein electrically connecting said flip-chip to said substrate comprises electrically connecting said flip-chip to said substrate with solder balls.

34. (previously presented) The method of claim 28, further comprising covering said flip-chip with an encapsulant.

35. (Canceled))

36. (previously presented) The method of claim 28, wherein electrically connecting said semiconductor die to said at least one of a plurality of shelves comprises electrically connecting a CPU chip to said at least one of said plurality of shelves.

37. (previously presented) The method of claim 28, wherein electrically connecting said flip-chip to said substrate comprises electrically connecting a memory cache flip-chip to said substrate.

38. (previously presented) The method of claim 28, wherein electrically connecting said semiconductor die to at least one of said plurality of shelves comprises electrically connecting said semiconductor die to said at least one of a plurality of shelves with at least one bond wire.

39. (Currently amended) ~~The method of claim 28, further including attaching said semiconductor die to a slug~~. The method of claim 28 wherein attaching said semiconductor die to a slug comprises attaching said semiconductor die to a slug comprising copper.

40. (Canceled)